Tanta University	**Second Term – Final Exam**
Faculty of Engineering	**Subject: Computer Architecture**
Computer and Control Dep.	**Allowed Time: 3 Hours**
Second Year	**Date: June 02, 2012**

Answer the following questions and assume any missing data; the exam consists of 3 questions.

Question 1: [Computer Arithmetic] — 40 Marks

1. Design 8-bit carry look-ahead adder with minimum gate delay that adds x_{0-7} to y_{0-7} then produces s_{0-7} and c_8 assuming that the fan in of the logic gates is 6, then find the logic gate delay of s_7 and c_8 in each case. (10 Marks)
2. Multiplying 01110110× 11010010 using: (10 Marks)
   a. Booth Algorithm
   b. Bit pairing recording of multipliers
3. Proof that the non-restoring and restoring divisions algorithms are equivalent then suggest hardware circuit for 8-bit binary division and explain its operation. (10 Marks)
4. Use 32-bit IEEE standard for floating point numbers to represent the following numbers in binary: (10 Marks)
   a. $(+23.25)_{10}$
   b. $(-144.125)_{10}$
   c. ∞
   d. $(-0.010110 \times 2^{-126})_2$

Question 2: [Input/Output Organization] — 24 Marks

1. Discuss the sequence of events involved in handling an interrupt request from a single I/O device, then show how two or more simultaneous interrupt requests can be handled. (8 Marks)
2. Explain the handshake control signals of data transfer over asynchronous bus during an output operation. (8 Marks)
3. Design a centralized bus arbitration system that applies daisy chain between 4 I/O devices assuming that all control devices are active high. Then draw the time sequence of signals that transfer the bus mastership to device number 2. (8 Marks)

Question 3: [Basic Processing Unit] — 26 Marks

1. Design an interface circuit between the processor and a printer assuming that the computer has 32-bit address bus, 16-bit data bus, status flag bit is transferred over line D_{10} of the data bus, and address line A_{31} is used as control signal, then design the logic circuit that can generate the status flag bit properly. (10 Marks)
2. Why is the *Wait-for-memory-function-completed* step needed when the processor is reading from or writing to the main memory? (4 Marks)
3. Assume single-bus processor, find out the control sequence for executing the following instructions:
   a. Move R3, R1
   b. Increment R2
   c. Add R1, (R2)
   d. GoTo L1

   If the memory access time is twice the processor clock time and both the processor and the memory are controlled by the same clock, estimate the total execution time of each sequence. (12 Marks)

Good Luck

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